SRI SIVASUBRAMANIYA NADAR COLLEGE OF ENGINEERING

(An Autonomous Institution)
Kalavakkam – 603 110

SELF STUDY REPORT

1.2.1 New Courses Introduced

M.E. VLSI Design

Submitted to

The National Assessment and Accreditation Council

February 2024

Name of the Programme : M.E. VLSI Design

Number of New Courses introduced in the Academic Year 2022-23 (Regulation 2022) : 3 Courses

List of New Courses :

S. No.	Name of the Course	Course Code
1	Digital ASIC Design	PVL2161
2	Design Verification and Testing Laboratory	PVL2212
3	Internship with Seminar	PVL2316

Documentary Evidence :

- Academic Council (AC) – Minutes of the fifth AC meeting dated 06-08-2022 to consider and approve the new PG Regulations R2022 with the revisions incorporated.
- Board of Studies (BoS) – Minutes of the Board of Studies meeting dated 31-05-2022 to consider and approve the PG R2022 curriculum and syllabus for M.E. VLSI Design.
- Curriculum – Regulations R2022 and R2018 Curriculum for M.E. VLSI Design with the new courses highlighted.

Sri Sivasubramaniya Nadar College of Engineering
Kalavakkam-603110
(An Autonomous Institution, Affiliated to Anna University, Chennai)

Fifth Meeting of the Academic Council

Date &Time: 06.08.2022 (10.00 a.m. to 3.00 p.m.)

AGENDA

1. To consider and approve the new PG Regulations R2022 with the revisions incorporated.
2. To ratify the amendments made in the UG Regulations (R2021).
3. To consider and approve the curriculum and syllabi of I, II, III and IV semesters of all PG programs to be offered from the Academic year 2022-2023 onwards.
4. To consider and approve the syllabi for B.E Hons. track courses in EEE & ECE.
5. To ratify the amendments made in the MBA Regulations (R2021).
6. To ratify the changes in the curriculum and syllabi of MBA program to be offered from the Academic year 2022-2023 onwards.
7. Other items, if any, with the permission of the Chairman of the Academic Council.

Chairman
Academic Council

Sri Sivasubramaniya Nadar College of Engineering
Kalavakkam-603110
(An Autonomous Institution, Affiliated to Anna University, Chennai)

MINUTES OF THE FIFTH ACADEMIC COUNCIL MEETING

Date: 6th August 2022 **Time: 10.00 a.m.** **Venue: ECE Seminar Hall, SSNCE.**

The following members attended the meeting:

- Dr. V.E.Annamalai, Principal & Chairman, Academic Council, SSNCE
- Dr.S. Ramanagopal, Professor & Member Secretary, Academic Council, SSNCE.
- Dr.S.Sridhar, Professor & Head, Department of Information Science and Technology, CEG campus, Anna University, Chennai.**(A.U. Nominee)**
- Dr.M.Meenakshi, Professor& Head, Department of Electronics and Communication Engineering, CEG campus, A.U., Chennai.**(A.U. Nominee)**
- Dr.R.Vidhya Priya, Professor & Head, Department of Biomedical Engineering, PSG College of Technology, Coimbatore.**(A.U. Nominee)**
- Mr.N.Siva Sankaran, Chief Technical officer, Viruksa Manufacturing Solutions Pvt., Ltd., Chennai.
- Mr.G.D.Sharma, Beeline HR advisory, Chennai.
- Dr. P. Somasundaram, Professor & Head, Department of Electrical and Electronics Engineering, CEG campus, Anna University, Chennai.
- Dr.P. Gomathi Priya, Professor, Department of Chemical Engineering, Alagappa College of Technology, Chennai.
- Dr. S. Radha, Vice Principal, SSNCE.
- Dr.S.Narasimman, CoE, SSNCE
- Dr. K. Hariharanath, Director, SSN School of Management.
- Dr.V.Rajini, Professor & Head, EEE, SSNCE.
- Dr.P.Vijayalakshmi, Professor & Head, SSNCE.
- Dr.T.T.Mirnalinee, Professor & Head, CSE, SSNCE.
- Dr. Chandrabose Aravindan, Professor & Head, IT, SSNCE.
- Dr. K. Sathishkumar, Professor & Head, Chemical Engg., SSNCE.
- Dr.A.Kavitha, Professor & Head, BME, SSNCE.
- Dr. K.S.Vijay Sekar, Professor & Head, Mechanical Engg., SSNCE.
- Dr.N.Sivakumar. Professor & Head, Civil Engg., SSNCE.
- Dr. B. Praba, Professor & Head, Mathematics, SSNCE.
- Dr. Masilla Moses Kennedy, Professor & Head, Physics, SSNCE.
- Dr.V.S.Gayathri, Professor & Head, Chemistry, SSNCE.
- Dr.Martha Karunakar, Associate Prof. & Head, English, SSNCE.
- Dr.A.Jawahar, Professor/ECE,SSNCE.
- Dr.N.Venkateswaran, Professor & IQAC coordinator, SSNCE.
- Dr. R.Seyezhai, Professor/EEE, SSNCE.
- Dr.M.Suresh,Associate Professor/Mechanical, SSNCE.
- Dr.V. Balasubramanian, Associate Professor/CSE, SSNCE

Sri Sivasubramaniya Nadar College of Engineering
Kalavakkam-603110
(An Autonomous Institution, Affiliated to Anna University, Chennai)

The Chairman welcomed all the members and gave a brief introduction of the purpose of the meeting. The Member Secretary, after welcoming the Anna University Nominees and the other expert members, presented the changes proposed in the PG Regulation and amendments in UG Regulation. The points discussed in the meeting on the specific clauses are given below.

1. Publication by P G student need not be mandatory. If yes let them communicate to journals of repute or with conference conducted by professional bodies. Avoid internally run conferences.
2. Can data science be included as open elective?
3. If NPTEL credits are not available, can we have alternate subject? PSG does additional exam for credit conversion.
4. PO across all programs – at least common number of POs.
5. Mandatory 3 as PO, remaining as PSO.
6. Uniform number of program electives to be offered under each vertical.
7. Internship and seminar – remove 'and' substitute 'with'.
8. Advanced radiation system – remove advanced.
9. Pattern recognition – very old – replace by Machine learning.
10. ME CSE – list of electives "Web application development" and "Functional programming" can go into software engineering. Electives can be regrouped.
11. IT – Health care , sports & fin Tech - can we rename as application of analytics
12. Why not include AR/VR etc. at least one paper.
13. One exclusive programming course – include in elective list
14. Can we have one exclusive lab for elective subject? Theory integrated lab can be considered for inclusion.
15. In device design include safety aspects also.
16. In Medical Electronics, 'Internship' name should be brought in, for uniformity.
17. In Biomedical device design, validation is important. Design for six sigma etc. can be included (Try including in syllabus)
18. a) In Manufacturing Engineering Electives – SCM is not apt. Can we replace by subject like world class mfg or subjects that talk about how to manufacture. Jigs & Fixtures, Lean Mfg etc. Control plan mechanism
    b) Design for manufacturing – move to core.
19. Energy auditing can be included as value added course.
20. Professional readiness for innovation, Employability and Entrepreneurship [3 credit] for CSE, IT and ECE UG programme under EEC category to be included in the revision of regulation.
21. MBA: The subject application of Analytics can be renamed as 'Functional Analytics'
22. Python for business – can be changed as 'Tools for Business Analytics'
23. Digital Marketing can be added as value added course.

Sri Sivasubramaniya Nadar College of Engineering
Kalavakkam-603110
(An Autonomous Institution, Affiliated to Anna University, Chennai)

The suggestions made by the members of the academic council were accepted and the Chairman thanked all the members for their participation.

Dr.V.E.Annamalai
Chairman

Dr.S.Ramana Gopal
Member Secretary

Dr.S.Sridhar
HOD/IT, CEG

Dr.M.Meenakshi
.HOD/ECE, CEG.

Dr.R.Vidhyapriya
HOD/BME, PSG Tech.

Mr.N.Siva Sankaran
CTO, Viruksa Pvt., Ltd.

Mr. G.D.Sharma
Beeline HR Advisory

Dr.P.Somasundaram
Prof./EEE, CEG

Dr.P.Gomathi Priya 6/8/2022
Prof./Chemical, A.C.Tech.

Signature of Participants: (Internal Members)

1. Dr. S. Radha, Vice Principal, SSNCE
2. Dr.S.Narasimman, CoE, SSNCE.
3. Dr. K.Hariharanath, Director, SSN School of Management
4. Dr. V. Rajini, Prof. & Head, EEE.
5. Dr. P. Vijayalakshmi, Prof. & Head, ECE. 06/08/22
6. Dr. T.T.Mirnalinee, Prof. & Head, CSE. 6/8/22
7. Dr. Chandrabose Aravindan, Prof. & Head, IT. 06/08/2022
8. Dr. K. Sathish Kumar, Prof. & Head, Chemical. 6/8/22
9. Dr. A. Kavitha, Prof. & Head, BME. 6/8/22
10. Dr. K.S.Vijay Sekar, Prof. & Head, Mechanical.
11. Dr. N. Sivakumar, Prof. & Head, Civil. 6/8/2022

12. Dr. B. Praba, Prof.& Head, Mathematics.
13. Dr. Masilla Moses Kennedy, Professor & Head, Physics.
14. Dr. V.S. Gayathri, Prof. & Head, Chemistry.
15. Dr. Martha Karunkar, Asso. Prof. &Head, English.
16. Dr.N. Venkateswaran, IQAC coordinator, SSNCE.
17. Dr.A.Jawahar,Professor/ECE,SSNCE.
18. Dr. R. Seyezhai, Professor/EEE, SSNCE.
19. Dr.M.Suresh, Associate Professor/Mechanical, SSNCE.
20. Dr.V.Balasubramanian, Associate Professor/CSE,SSNCE

SSN/R2022/ECE/BoS-MoM

SSN College of Engineering

(An Autonomous Institution Affiliated to Anna University, Chennai)

Kalavakkam – 603110

The Minutes:

The meeting is called to consider the PG R2022 curriculum & syllabi, BE (Hons) and few amendments to UG R2021-Curriculum.

In attendance

1. Dr. P. Vijayalakshmi (Chair - Convener) - PV
2. Dr. D. Meganathan (University Nominee) - DM
3. Dr. Deepa Venkitesh (Academic Expert) - DV
4. Dr. Asuthosh Kar (Academic Expert) - AK
5. Mr. G. Kannan (Industrial Expert) - GK
6. Faculty members of the department of ECE.

In absentia (suggestions received through email)

1. Dr. K. Mourougayane (Industrial Expert) – KM
2. Mr. Karunadurai (Alumnus) - GCK

Discussions:

1. PV welcomed the gathering and introduced the external members to the faculty.
2. PV presented the features of the PG CS, Curriculum & Syllabi
3. PV highlighted that the POs we set in the perspective of independent learning.
4. PV mentioned that industry inputs are considered for a minimum of two courses for the all the three programs.
5. DV suggested making Research Methodology and IPR course a Pass/Fail course.
6. A discussion was held on the duration of internship as part of the course “Internship and Seminar”. The discussion was initiated by DV and as anindustry expert GK suggested to have atleast 6 to 8 weeks. Final consensusof the discussion was to have at least 8 weeks of internship to have a meaningful outcome for both the stake holders, students and industry.

Considering the logistics it was proposed to move the course from Semester II to Semester III.

7. AK suggested to include two additional experiments (in buffer) in each lab for all the three programs
8. DV suggested to allow students to take an NPTEL course in place of one ofthe professional electives. This proposal will be taken forward for feasibility.
9. A discussion was initiated to allocate more time for the research as part of theproject in semester III upon agreement suggested in point 5.
   The course research methodology and IPR if made as a PASS/FAIL course, it would release 2 credits in Semester I. One of the core courses from Semester II is shifted to Semester I, increasing the number of credits in Semester I to 19. Concurrently, one of the professional electives from Semester III is shifted to Semester II.
   The 2 credits for research methodology and IPR is distributed to all the four lab courses equally.
   The total number of credits remain unchanged.

M.E – Communication Systems

10. A discussion was initiated by GK, AK and DV on the content of both Mathematical Foundation course and Advanced Digital Signal Processing (ADSP). The consensus was to move ADSP from semester I to semester II and Advanced Wireless Networks from Semester II to Semester I. Considering the logistics the Signal processing component of the Communication and Signal processing lab was moved to semester II.
11. DV highlighted the redundancy of the word “advanced” in many subjects. After discussion the word advanced was dropped and the course titles were modified for the following courses: (i) “Advanced Radiating Systems” as Radiating Systems, (ii) “Advanced Wireless Networks” as “Communication System Networks”, and (iii) “Advanced Optical Communication” as “Fibre Optic Communication Technologies” Advanced Signal Processing as “Statistical Signal Processing”.
12. A common suggestion of providing the electives as combined list to increase the freedom of choosing a particular pathway for the students was initiated by DV and a common consensus was arrived to have a unified elective list.
13. The following courses were suggested by DV, GK and AK to be included in the elective list: Digital modulation and coding, Information Theory, signal detection and estimation.
14. A few additional topics were suggested to be included by the expert members. These were noted down and will suitably be accommodated.
15. A suggestion was made by AK to explore the possibility of converting the course Pattern Recognition, a 3 credit theory course to 4 credit theory cum practical course.
16. PV summarized the suggestions.

M.E – Applied Electronics

17. PV presented the PG AE Curriculum & Syllabi.

18. The following courses were suggested by DV, GK and AK to be included in the elective list: Python programming, RF energy harvesting and ARM-based development, Battery technologies.

19. A suggestion was initiated by DV and GK regarding the title and content of "Advanced microcontroller" course. The consensus after the discussion was to rename the course as Microcontrollers and Interfacing. The topics that need to be included / revised are captured in the addendum.

20. A few additional topics were suggested to be included by the expert members. These were noted down and will suitably be accommodated.

21.A revision of the following course titles was suggested by GK, AK and DV :

(i) "Medical Embedded System" as "Embedded System for Health Care",

(ii) "Embedded Networking" as "Embedded System Development"

(iii) "VLSI Technology" to "CMOS Fabrication Technology".

22. AJ (Dr. A. Jawahar) summarized the suggestions.

M.E – VLSI Design

23. PV presented the PG VLSI Curriculum & Syllabi.

24. A suggestion was made by DM to explore the possibility of converting the course Digital ASIC Design, a 3 credit theory course to 4 credit theory cum practical course.

25. To accommodate the suggestion made in point 24, the following changes may be made.

i. CMOS Analog IC design & CMOS Analog IC design lab from semester II to semester I, and VLSI Physical Design Algorithm from semester I to semester II.

ii. PVC and VV proposed to introduce RF IC design laboratory in semester II as a new laboratory course.

26. A few additional topics were suggested to be included by the expert members. These were noted down and will suitably be accommodated.

27. The following courses were suggested by DV, GK and DM to be included inthe elective list:(i) Network-on-Chip (ii) RF energy harvesting and (iii) Multicore Architectures

28. PVC (Dr. Premanand) summarized the suggestions.

BE Honours Program

29. PV briefed about the BE honours degree as per R2021 and detailed the additional credits (6 new courses) and the syllabi of BE (Hons).

The following are the new courses

- Embedded Programming
- IoT Architectures
- IoT Communication Technologies

- Data Science for IoT
- Security and Privacy in IoT
- Industrial IoT 4.0
- Mini Project in IoT

30. GK suggested to include Aadhar Based Authentication in the course Security and Privacy in IoT

Amendments in UG R 2021 Curriculum

31. PV presented the amendments for UG R2021 regulations based on the concerns received from the course instructors and coordinators of respective courses. The following amendments were discussed and agreed by the members.

- Fundamentals of Electronic Devices and Circuits: the number of mini projects to be implemented is reduced from 6 to 2.
- DSP Lab: processor based experiments are revised as MATLAB based experiments.
- System Design for IoT: Unit III revised and relevant Text book included.

32. PV thanked and the meeting adjourned at 3:15pm.

Addendum

1. The following suggestions were given by GK in ME CS Syllabi

- Suggested removing WiMAX in AWC while including Wi-Fi.
- Suggested introducing FSO in the syllabus because it is going to be a major part of 6G communication.
- Suggested introducing non-idealities in Communication systems can be taken up in the lab for measurements.
- Suggested that one unit can be allotted for Math modelling of non-linearity in MIC course.
- Suggested to include the MLSE, RLS filter and Kalman Filter in Advanced Signal Processing Course.

2. The following suggestions were given in the content of ME AE syllabi.

- DM suggested adding universal verification methodology, the concept of controllability and observability in Advanced Digital System Design.
- KM suggested to include the following topics in various subjects, Advanced Digital System Design — Unit V: Timing Analysis and concepts of model-based design can be added

Sensors, Actuators and System Interface — Unit V: Sensors for body area networks can be added
Automotive Electronics - Unit V: Safety interlocks can be added
Design Automation Lab — Traffic signal automation and Body area network automation cane be added

- GCK suggested to include the following in the Embedded System Lab experiments,
  Design an Adaptive Cruise Control (ACC) System
  Design a biomedical lab system
- GK recommended to include GPS (NAVIC) and usage of Kalman filters for IMU in Unit 1 and 2 of Sensors, Actuators and System Interface.
- GK suggested including Linux and device kernel architectures and drivers for both theory and lab of embedded system design. He insisted to generalize the course outcome as operating system rather than mentioning specifically RTOS.
- AK and DV suggested to have a few more extra experiments for all the lab courses throughout all the branches as a buffer to increase the leverage in choosing experiments of interest.
- DM suggested including DCVSL, timing issues and pass transistorlogic in CMOS digital VLSI design.
- MR suggested to include safety interlocks in unit 5 of Automotive Electronics.
- DM suggested to provide wide options in EDA tools instead of restricting to cadence. GK commented as the students should be encouraged to use both open sources as well as commercially available EDA tools.
- DM suggested to include BSIM and EKV models in MOS device modelling
- DM suggested to include a resistive divider and comparator in Data converters.
- DM suggested including the introduction of field-programmable analog array in unit 5 of Reconfigurable VLSI Architecture
- GK and DV suggested considering a specific microprocessor and elaborating all the peripherals in advanced microcontroller and interfacing. He insisted to include security concepts in unit 5 and rename the course accordingly.
- GK suggested including correlation concepts in unit 3 of signal processing for VLSI and he mentioned to consider differentiating correlation from filters
- DV, GK and AK suggested having practical component in the courses Advanced Computer Organization and Architecture, Advanced Microcontroller and Interfacing, Deep Learning and Soft Computing Techniques.
- GK insisted to include PCB stacking and network matching in signal integrity for high-speed design.

3. The following suggestions were given by the members in ME VLSI syllabi.

- GK suggested to add computational complexity theory in VLSI Physical Design and Algorithms course
- KM suggested to include the following topics in various subjects,
  VLSI Physical design and algorithms – UNIT V: can cover a case study on physical design
  RF IC Design — UNIT V: Transceiver design considerations withrespect to single chip and two chip case study
  Design, Verification and Testing Lab: One experiment with shift register can be added
  Signal Integrity for IC speed design: Unit V: Mixed signal design considerations, multilayer PCB design practice can be added
- DM suggested including of the following topics; DCVSL logic, pass transistor logic in Unit 3 and timing issues & Memories in Unit 4 of CMOS digital VLSI design course.
- DM and GK suggested to add the following topics; open circuit time constant, Zero value time constant, Bandwidth constant and Miller compensation in CMOS Analog IC design course.
- DM suggested to explore FPAA to analyse the analog components

SSN College of Engineering

(An Autonomous Institution Affiliated to Anna University, Chennai)

Kalavakkam – 603110

Signature of Internal Members

Sl.NO	STAFF NAME	Designation	Signature
1.	Dr. PREMANAND CHANDRAMANI	Prof.	
2.	Dr. R.AMUTHA	Prof.	
3.	Dr. N.VENKATESWARAN	Prof.	
4.	Dr. R.JAYAPARVATHY	Prof.	
5.	Dr. K.T.SELVAN	Prof.	
6.	Dr. A.JAWAHAR	Prof.	
7.	Dr. N.EDNA ELIZABETH	Prof.	
8.	Dr. R.RAJAVEL	Asso.Prof.	
9.	Dr. R.KISHORE	Asso. Prof.	
10.	Dr. B.S.SREEJA	Asso. Prof.	
11.	Dr. K. S.VISHVAKSENAN	Asso. Prof.	
12.	Dr. K.MUTHUMEENAKSHI	Asso. Prof.	
13.	Dr. S.SAKTHIVEL MURUGAN	Asso. Prof.	
14.	Dr. R.KALIDOSS	Asso. Prof.	
15.	Dr. M.GULAM NABI ALSATH	Asso. Prof.	
16.	Dr. S.ESTHER FLORENCE	Asso. Prof.	
17.	Dr. K.J.JEGADISH KUMAR	Asso. Prof.	
18.	Dr. V.VAITHIANATHAN	Asso. Prof.	
19.	Dr. K.K.NAGARAJAN	Asso. Prof.	
20.	Dr. R.HEMALATHA	Asso. Prof.	
21.	Dr. M.ANBUSELVI	Asso. Prof.	
22.	Dr.C.ANNADURAI	Asso. Prof.	
23.	Dr. B.RAMANI	Asso. Prof.	
24.	Dr. B.PARTIBANE	Asso. Prof.	
25.	Dr. S.RAMPRABHU	Asso. Prof.	
26.	Dr. I.NELSON	Asso. Prof.	
27.	Dr. W.JINO HANS	Asso. Prof.	
28.	Dr. S.KIRUBAVENI	Asso. Prof.	
29.	Dr. N.PRABAGARANE	Asso. Prof.	

SSN College of Engineering

(An Autonomous Institution Affiliated to Anna University, Chennai)

Kalavakkam – 603110

30.	Dr. P.KAYTHRY	Asso. Prof.	
31.	Dr. G.DURGA	Asso. Prof.	
32.	Dr. C.VINOTH KUMAR	Asso. Prof.	
33.	Dr. S.KARTHIE	Asso. Prof.	
34.	Dr. S.HANIS	Asso. Prof.	

SSN College of Engineering

(An Autonomous Institution Affiliated to Anna University, Chennai)

Kalavakkam – 603110

Dr.P. Vijayalakshmi 31/05/22
Professor & Head,
Department of Electronics and
Communication Engineering,
SSN College of Engineering.
Chairman,
BoS for Electronics and
Communication Engineering

Dr. D. Meganathan 31/5/22
Associate Professor
Department of ElectronicsEngineering
MIT Campus, Anna University, Chennai.
University Nominee

Dr.Deepa Venkitesh
Professor
Department of Electrical Engineering
Indian Institute of Technology Madras,
Chennai
Academic Expert

31/05/2022
Dr. Asuthosh Kar
Assistant Professor (senior grade)
Indian Institute of Information
Technology,
Design and Manufacturing (IIITDM)
Kanchipuram
Academic Expert

Dr. K. Mourougayane
Scientist F & Head – DSP Division
Society for Applied Microwave
Electronics Engineering &Research (SAMEER)
Centre for Electromagnetics (CEM)
CIT Campus, Tharamani, Chennai
Industrial Expert

31/5/22.
Mr. G. Kannan
Managing Director
BigCAT Wireless Private Ltd.,
IIT Madras Research Park,
Tharamani, Chennai
Industrial Expert

Mr. Karunadurai GC
Technical Architect
Continental Automotive, Bangalore
Alumnus

Sri Sivasubramaniya Nadar College of Engineering

(An Autonomous Institution, Affiliated to Anna University, Chennai)

Rajiv Gandhi Salai (OMR), Kalavakkam – 603110

Regulations 2022

Curriculum and Syllabi for

Master of Engineering

in

VLSI Design

Vision and Mission of the Department

Vision:

To be in a position of enhanced national and global reputation as a department offering excellent educational programmes and undertaking internationally recognized research and development activities in electronics and communication engineering

Mission:

- Continued focus on excellence in teaching and learning by investing in faculty and staff development and resources.
- Promoting an all-round development of our students through curricular and co-curricular activities that instil a spirit of social responsibility, innovation, creativity and entrepreneurship.
- Attracting a larger number of the best students at both the graduate and undergraduate level
- Promoting high-quality research leading to publications in reputed journals and patents.
- Building partnerships with leading academic institutions and industries.
- Nurturing a learning and work environment that makes the department one of the best ECE communities for students, faculty and staff.

Programme Educational Objectives

PEO1 (Professional development): Graduates will have a successful career in VLSI system design or associated industries or research and higher education, or as entrepreneurs.

PEO2 (Attitude towards lifelong-learning): Graduates will have the ability and attitude to adapt the evolving technological changes.

Programme Outcomes

Engineering Graduates will be able to:

PO1: An ability to independently carry out research / investigation and development work to solve practical problems.
PO2: An ability to write and present a substantial technical report/document.
PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PO4: Design and develop solutions for problems in digital and analog electronic system through VLSI Integrated Circuits.
PO5: Execute independently the projects involving simulations and / or measurements in digital and analog electronic circuits and system design.

Mapping of Programme Educational Objectives with Programme Outcomes:

The correlation between the defined POs and the PEOs is given in Table 1

Table 1: Correlation between the defined POs and the PEOs

PEOs	POs				
	PO1	**PO2**	**PO3**	**PO4**	**PO5**
PEO01	3	3	3	2	3
PEO02	2	3	2	2	2

Mapping Criterion: Strong - 3 Significant - 2 Reasonable - 1

Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam - 603110
(An Autonomous Institution, Affiliated to Anna University, Chennai)
ME in VLSI Design
REGULATIONS – 2022
CHOICE BASED CREDIT SYSTEM

MAPPING OF COURSE OUTCOMES WITH PROGRAMME OUTCOMES

A broad relation between the Course Outcomes and Programme Outcomes is given in the following table

COURSE OUTCOMES		PROGRAMME OUTCOMES				
Sem	**Course Name**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**
	Programme Core					
I	Applied Mathematics for VLSI Design			3		
	Digital ASIC Design	2	2	3	3	2
	CMOS Analog Integrated Circuit Design	1	1	2.8	3	1
	CMOS Digital VLSI Design	1	1	3	3	1
	VLSI Physical Design and Algorithms	1	1	3	3	1
	Research Methodology & IPR					
	Practicals					
	CMOS Analog IC Design Laboratory	3	3	3	3	3
	CMOS Digital VLSI design Laboratory	3	3	3	3	3
	Audit Course					
	English for Research paper writing					
	Disaster Management					
	Value Education					
	Pedagogy Studies					
	Personality Development through life enlightenment skills					
	Constitution of India					
	Programme Core					
	RF IC Design	1	1	3	2.8	1
	Design for Testability	1	1	3	3	1
	Programme Elective I					

	MEMS and NEMS	1	1	3	3	1
	Nano Electronics and Technology	1	1	3	2	
	Nanoscale Transistors	1	1	3	2.2	
	Pattern Recognition and Machine Learning	1	1	3	3	1
	Embedded System Programming	1.4	2	2	2	2
	Programme Elective II					
	Data Converters	1	1	3	3	1
	Signal Integrity for High-Speed Design	2	1	3	2	
	RF and Microwave Circuit Design	1.75		2.75	2.5	1.75
	Robotics and Automation	1	1	3	1.8	1
	ARM Based Development	1.4	2	2	2	2
	Programme Elective III					
	Hardware Software Co-Design	1	1	3	2	1
	Signal Processing for VLSI	1	1	2.8	2.8	1
	Advanced Computer Organization and Architecture	1	1	3	2	1
	System on Chip Design	1	1	3	2	
	Multi-core architecture and programming	1.4	2	2	2	2
	Practicals					
	RF IC Design Laboratory	2	2	3	3	3
	Design Verification and Testing Laboratory	3	3	3	3	3
	Programme Elective IV					
	Low Power VLSI Design	1	1	3	3	
	MOS Device Modelling	1	1	3	2	1
	CMOS Fabrication Technology	1	1	3	2	
III	Embedded System Design	2	1	3	2	
	RF energy harvesting	3	3	1	1	1
	Programme Elective V					
	Reconfigurable VLSI Architectures	1	1	3	3	1
	Deep Learning Techniques	1	2	3	2	1.333

	Machine Vision	1	1	2.8	2.2	1
	Sensors, Actuators and System Interface	2	2	3	2.8	
	Network-On-Chip	2	2	1	1	1
	Open Elective					
	Business analytics					
	Industrial Safety					
	Operations Research					
	Cost Management of Engineering Projects					
	Composite Materials					
	Waste to Energy					
	Introduction to Data Science					
	Employability Enhancement Course - I					
	Internship with Seminar					
	Project Phase I					
IV	**Employability Enhancement Course - II**					
	Project Phase II					

Mapping Criterion: Strongly agree - 3 Agree - 2 Weakly agree - 1

Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam - 603110
(An Autonomous Institution, Affiliated to Anna University, Chennai)

M.E – VLSI Design
I to IV semesters Curriculum - R 2022 (Choice Based Credit System)

SEMESTER I								
Sl. No.	**COURSE CODE**	**COURSE TITLE**	**CATEGORY**	**CONTACT PERIODS**	**L**	**T**	**P**	**C**
THEORY								
1	PMA2155	Applied Mathematics for VLSI Design	PC	3	3	0	0	3
2	PVL2161	Digital ASIC Design	PC	5	3	0	2	4
3	PVL2101	CMOS Analog Integrated Circuit Design	PC	3	3	0	0	3
4	PVL2102	CMOS Digital VLSI Design	PC	3	3	0	0	3
5	PVL2103	VLSI Physical Design and Algorithms	PC	3	3	0	0	3
6	PGE2176	Research Methodology & IPR	MLC	2	2	0	0	2
7		Audit Course	AC	2	2	0	0	0
PRACTICALS								
8	PVL2111	CMOS Analog IC Design Laboratory	PC	4	0	0	4	2
9	PVL2112	CMOS Digital VLSI design Laboratory	PC	4	0	0	4	2
			TOTAL	**29**	**19**	**0**	**10**	**22**

PC - Programme Core, MLC - Mandatory Learning Course, AC - Audit Course

SEMESTER II								
Sl. No.	**COURSE CODE**	**COURSE TITLE**	**CATEGORY**	**CONTACT PERIODS**	**L**	**T**	**P**	**C**
THEORY								
1	PVL2201	RF IC Design	PC	3	3	0	0	3
2	PVL2202	Design for Testability	PC	3	3	0	0	3
3		Programme Elective I	PE	3	3	0	0	3
4		Programme Elective II	PE	3	3	0	0	3
5		Programme Elective III	PE	3	3	0	0	3
PRACTICALS								
6	PVL2211	RF IC Design Laboratory	PC	4	0	0	4	2
7	PVL2212	Design Verification and Testing Laboratory	PC	4	0	0	4	2
			TOTAL	**23**	**15**	**0**	**8**	**19**

PE - Programme Elective

SEMESTER III								
Sl. No.	**COURSE CODE**	**COURSE TITLE**	**CATEGORY**	**CONTACT PERIODS**	**L**	**T**	**P**	**C**
THEORY								
1		Programme Elective IV	PE	3	3	0	0	3
2		Programme Elective V	PE	3	3	0	0	3
3		Open Elective	OE	3	3	0	0	3
PRACTICALS								
4	PVL2316	Internship with Seminar	EEC	4	0	0	4	2
5	PVL2318	Project Phase I	EEC	12	0	0	12	6
			TOTAL	**25**	**9**	**0**	**16**	**17**

OE - Open Elective, EEC - Employability Enhancement Course

SEMESTER IV								
Sl. No.	**COURSE CODE**	**COURSE TITLE**	**CATEGORY**	**CONTACT PERIODS**	**L**	**T**	**P**	**C**
PRACTICALS								
1	PVL2418	Project Phase II	EEC	24	0	0	24	12
			TOTAL	**24**	**0**	**0**	**24**	**12**

Total Credits: 70

SUMMARY

DISTRIBUTION OF CREDITS

Sl. No	**Category**	**Credits as per Semester**				**Total Credits**	**Percentage**
		I	**II**	**III**	**IV**		
1	**PC**	20	10			30	42.86
2	**PE**		9	6		15	21.43
3	**EEC**			8	12	20	28.57
4	**MLC**	2				2	2.85
5	**OE**			3		3	4.29
Total						**70**	**100**

CATEGORY WISE LISTING OF COURSES

PROGRAMME CORE (PC)

Sl. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	PMA2155	Applied Mathematics for VLSI Design	PC	3	3	0	0	3
2	PVL2161	Digital ASIC Design	PC	5	3	0	2	4
3	PVL2101	CMOS Analog Integrated Circuit Design	PC	3	3	0	0	3
4	PVL2102	CMOS Digital VLSI Design	PC	3	3	0	0	3
5	PVL2103	VLSI Physical Design and Algorithms	PC	3	3	0	0	3
6	PVL2111	CMOS Analog IC Design Laboratory	PC	4	0	0	4	2
7	PVL2112	CMOS Digital VLSI design Laboratory	PC	4	0	0	4	2
8	PVL2201	RF IC Design	PC	3	3	0	0	3
9	PVL2202	Design for Testability	PC	3	3	0	0	3
10	PVL2211	RF IC Design Laboratory	PC	4	0	0	4	2
11	PVL2212	Design Verification and Testing Laboratory	PC	4	0	0	4	2

PROGRAMME ELECTIVES (PE)

SEMESTER II

PROGRAMME ELECTIVE I

Sl. No.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1	PAE2246	MEMS and NEMS	PE	3	3	0	0	3
2	PAE2241	Nano Electronics and Technology	PE	3	3	0	0	3
3	PVL2221	Nanoscale Transistors	PE	3	3	0	0	3
4	PCN2244	Pattern Recognition and Machine Learning	PE	3	3	0	0	3
5	PAE2247	Embedded System Programming	PE	3	3	0	0	3

PROGRAMME ELECTIVE II

Sl. No.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1	PVL2242	Data Converters	PE	3	3	0	0	3
2	PCN2241	Signal Integrity for High-Speed Design	PE	3	3	0	0	3
3	PCN2201	RF and Microwave Circuit Design	PE	3	3	0	0	3
4	PAE2202	Robotics and Automation	PE	3	3	0	0	3
5	PAE2245	ARM Based Development	PE	3	3	0	0	3

PROGRAMME ELECTIVE III

Sl. No.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1	PAE2243	Hardware Software Co-Design	PE	3	3	0	0	3
2	PVL2241	Signal Processing for VLSI	PE	3	3	0	0	3
3	PAE2244	Advanced Computer Organization and Architecture	PE	3	3	0	0	3
4	PAE2248	System-on-Chip Design	PE	3	3	0	0	3
5	PVL2222	Multi-core architecture and programming	PE	3	3	0	0	3

SEMESTER III

PROGRAMME ELECTIVE IV

Sl. No.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1	PVL2342	Low Power VLSI Design	PE	3	3	0	0	3
2	PVL2341	MOS Device Modelling	PE	3	3	0	0	3
3	PVL2343	CMOS Fabrication Technology	PE	3	3	0	0	3
4	PAE2103	Embedded System Design	PE	3	3	0	0	3
5	PAE2342	RF energy harvesting	PE	3	3	0	0	3

PROGRAMME ELECTIVE V

Sl. No.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1	PVL2344	Reconfigurable VLSI Architectures	PE	3	3	0	0	3
2	PCN2342	Deep Learning Techniques	PE	3	3	0	0	3
3	PCN2341	Machine Vision	PE	3	3	0	0	3
4	PAE2102	Sensors, Actuators and System Interface	PE	3	3	0	0	3
5	PAE2341	Network-on-chip	PE	3	3	0	0	3

EMPLOYABILITY ENHANCEMENT COURSE (EEC)

Sl. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	PVL2316	Internship with Seminar	EEC	4	0	0	4	2
2	PVL2318	Project Phase I	EEC	12	0	0	12	6
3	PVL2418	Project Phase II	EEC	24	0	0	24	12

MANDATORY LEARNING COURSES (MLC)

Sl. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	PGE2176	Research Methodology & IPR	MLC#	2	2	0	0	2

AUDIT COURSES (AC)

Sl. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	AGE2001	English for Research paper writing	AC	2	2	0	0	0
2	AGE2002	Disaster Management	AC	2	2	0	0	0
3	AGE2003	Value Education	AC	2	2	0	0	0
4	AGE2004	Pedagogy Studies	AC	2	2	0	0	0
5	AGE2005	Personality Development through life enlightenment skills	AC	2	2	0	0	0
6	AGE2006	Constitution of India	AC	2	2	0	0	0

OPEN ELECTIVE COURSES (OE)

Sl. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	PGE2941	Business analytics	OE	3	3	0	0	3
2	PGE2942	Industrial Safety	OE	3	3	0	0	3
3	PGE2943	Operations Research	OE	3	3	0	0	3
4	PGE2944	Cost Management of Engineering Projects	OE	3	3	0	0	3
5	PGE2945	Composite Materials	OE	3	3	0	0	3
6	PGE2946	Waste to Energy	OE	3	3	0	0	3
7	PGE2947	Introduction to Data Science	OE	3	3	0	0	3

Sri Sivasubramaniya Nadar College of Engineering

(An Autonomous Institution, Affiliated to Anna University, Chennai)

Rajiv Gandhi Salai (OMR), Kalavakkam – 603110

Curriculum and Syllabus

Master of Engineering
VLSI Design

Regulations 2018

Choice Based Credit System (CBCS)

Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam - 603110
(An Autonomous Institution, Affiliated to Anna University, Chennai)

Vision and Mission of the Department

Vision:

To develop centres of excellence in the field of Electronics &Communication Engineering and produce outstanding & meritorious engineers

Mission:

- To design innovative and comprehensive instructional material for facilitating enhanced student learning.
- To infuse scientific temper in the students and guide them to produce exemplary research
- To cultivate a committed group of competent faculty striving for excellence in teaching and research
- To develop collaborative research and linkages with leading organizations in India and abroad
- To nurture talent and foster entrepreneurial & social spirit among students

Program Educational Objectives (PEOs):

PEO1: Professional development: Graduates will have a successful career in communication system design or associated industries or research and higher education, or as entrepreneurs

PEO2: Attitude towards lifelong-learning: Graduates will have the ability and attitude to adapt to evolving technological challenges

Program Outcomes:

Upon completion of the Programme, Graduates will

a) **Scholarship of Knowledge**: Acquire in-depth knowledge in Electronics & VLSI system design with an ability to understand, apply, analyze and integrate the same for enhancement of knowledge.

b) **Critical Thinking**: Analyze engineering problems in Electronics and VLSI system design and evaluate independently to make intellectual and/or creative choices for conducting research.

c) **Problem Solving**: Identify, analyze and develop optimal solutions to solve Electronics and VLSI system design problems, and understand its impact on the society.

d) **Research Skill**: Extract information through literature survey, apply appropriate methodologies, conduct experiments, analyze and interpret data individually or in group(s) for enhancement of knowledge in Electronics and VLSI system design.

e) **Usage of modern tools**: Use appropriate techniques, and modern engineering tools, for Electronics and VLSI system design.

f) **Collaborative and Multidisciplinary work**: Demonstrate an ability to visualize and contribute to collaborative-multidisciplinary research, as an individual or as a member of a team.

g) **Project Management and Finance**: Apply the engineering and management principles for efficient project management.

h) **Communication**: Comprehend and communicate confidently and effectively in both verbal and written form.

i) **Life-long Learning**: Recognize the need and acquire confidence for independent and life-long learning.

j) **Ethical Practices and Social Responsibility**: Acquire knowledge of professional and ethical responsibilities.

k) **Independent and Reflective Learning**: Observe and examine the outcomes of one's actions and take independent corrective measures**.**

Mapping of Programme Educational Objectives with Department Mission:

Table 1: Mapping of PEOs with Mission of the Department

Mission	PEO1	PEO2
To design innovative and comprehensive instructional material for facilitating enhanced student learning	**3**	**3**
To infuse scientific temper in the students and guide them to produce exemplary research	**2**	**3**
To cultivate a committed group of competent faculty striving for excellence in teaching and research	**2**	**2**
To develop collaborative research and linkages with leading organizations in India and abroad	**3**	**3**
To nurture talent and foster entrepreneurial & social spirit among students	**3**	**3**

Mapping Criterion: Strong - 3 Significant - 2 Reasonable - 1

Mapping of Programme Educational Objectives with Programme Outcomes:

The correlation between the defined POs and the PEOs is given in Table

Table 2: Correlation between the defined POs and the PEOs

PEOs	Graduate Attributes/POs										
	a	**b**	**c**	**d**	**e**	**f**	**g**	**h**	**I**	**j**	**k**
PEO1	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**3**	**3**
PEO2	**3**	**3**	**3**	**3**	**2**	**2**	**2**	**3**	**3**	**3**	**3**

Mapping Criterion: Strong - 3 Significant - 2 Reasonable - 1

Mapping of Programme Outcomes with Graduate Attributes:

Table 3: Mapping of Programme Outcomes with NBA Graduate Attributes

Programme Outcomes	NBA's GAs
a) **Scholarship of Knowledge**: Acquire in-depth knowledge in Electronics & VLSI system design with an ability to understand, apply, analyze and integrate the same for enhancement of knowledge	GA1
b) **Critical Thinking**: Analyze engineering problems in Electronics and VLSI system design and evaluate independently to make intellectual and/or creative choices for conducting research	GA2
c) **Problem Solving**: Identify, analyze and develop optimal solutions to solve Electronics and VLSI system design problems, and understand its impact on the society	GA3

d) **Research Skill**: Extract information through literature survey, apply appropriate methodologies, conduct experiments, analyze and interpret data individually or in group(s) for enhancement of knowledge in Electronics and VLSI system design	GA4
e) **Usage of modern tools**: Use appropriate techniques, and modern engineering tools, for Electronics and VLSI system design	GA5
f) **Collaborative and Multidisciplinary work**: Demonstrate an ability to visualize and contribute to collaborative-multidisciplinary research, as an individual or as a member of a team	GA6
g) **Project Management and Finance**: Apply the engineering and management principles for efficient project management	GA7
h) **Communication**: Comprehend and communicate confidently and effectively in both verbal and written form	GA8
i) **Life-long Learning**: Recognize the need and acquire confidence for independent and life-long learning	GA9
j) **Ethical Practices and Social Responsibility**: Acquire knowledge of professional and ethical responsibilities	GA10
k) **Independent and Reflective Learning**: Observe and examine the outcomes of one's actions and take independent corrective measures	GA11

Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam - 603110

(An Autonomous Institution, Affiliated to Anna University, Chennai)

M.E. in VLSI DESIGN

REGULATIONS – 2018

CHOICE BASED CREDIT SYSTEM

MAPPING OF COURSE OUTCOMES WITH PROGRAMME OUTCOMES:

A broad relation between the Course Outcomes and Programme Outcomes is given in the following table

Sem	COURSE OUTCOMES		PROGRAMME OUTCOMES										
	Course Name		a	b	c	d	e	f	g	h	i	j	k
I	Advanced Applied Mathematics		3	2	2	2	0	0	0	0	0	0	2
	Digital CMOS VLSI Design		3	2	2	2	1	1	0	0	0	0	0
	Advanced Digital System Design		3	3	3	1	2	0	0	1	0	0	0
	Analog Integrated Circuit Design		3	3	3	2	2	0	0	1	0	0	0
	Solid State Devices and Integrated Circuits - I		3	3	2	1	1	0	0	1	1	1	0
	DSP Integrated Circuits		3	3	3	3	2	2	1	0	0	0	0
	Integrated Circuits Laboratory		3	3	3	3	3	2	2	2	2	1	1
	Technical Seminar		3	3	0	2	3	0	0	3	2	2	3
II	Hardware Software Co-Design		3	3	2	3	3	2	1	2	3	2	1
	VLSI Physical Design and Algorithms		3	3	3	3	3	2	2	2	2	1	1
	Design for Testability		3	3	3	2	1	1	0	0	0	0	0
	Professional Elective - I	VLSI System Design	3	2	2	3	1	0	0	0	0	0	0
		Data Converters	3	3	3	2	2	0	0	1	0	0	0
		Signal Integrity for High Speed Design	3	3	3	3	3	1	1	1	2	1	1
		Microwave Integrated Circuits	3	2	3	3	3	1	2	1	1	1	2
	Professional Elective - II	Embedded System Design for IoT	3	3	2	3	2	3	2	2	2	2	2
		Multimedia compression techniques	3	2	3	3	1	0	0	0	1	0	0
		Software Defined Radio	3	3	3	1	2	1	1	2	2	1	1
		Cryptography and Network Security	3	3	3	3	2	3	1	1	3	2	1
	Professional Elective - III	MEMS and NEMS	1	3	2	3	3	3	1	1	1	1	2
		Nano Electronics and Technology	3	2	2	1	2	2	1	2	1	1	1

Sem	COURSE OUTCOMES		PROGRAMME OUTCOMES										
	Course Name		a	b	c	d	e	f	g	h	i	j	k
		DSP processor architecture and programming	2	3	2	3	3	3	1	1	1	1	1
		Advanced Digital Image Processing	2	3	3	3	3	3	1	1	2	1	1
	VLSI System Design Laboratory		3	3	3	3	3	2	2	2	2	1	1
	Technical Writing		3	3	0	2	3	0	0	3	2	2	3
III	Professional Elective -IV	Advanced Computer Organization and Architecture	3	2	2	2	2	0	0	0	0	0	0
		CAD for VLSI IC Design	3	2	2	2	1	0	0	0	0	0	0
		RF IC Design	3	3	3	2	2	0	0	1	0	0	0
		Low Power VLSI Design	3	2	2	2	3	1	0	0	0	3	2
	Professional Elective -V	Scripting Languages for VLSI	1	1	2	2	2	1	0	0	0	0	0
		VLSI Technology	3	2	2	2	1	1	0	0	0	0	0
		Nano Scale Transistors	3	3	2	2	1	0	0	1	1	0	1
		Sensors, Actuators and System Interface	3	3	2	3	1	2	1	2	3	1	2
	Professional Elective -VI	Artificial Intelligence	3	3	2	1	1	1	0	1	1	0	1
		Quantum Computing and Quantum Information	3	3	2	2	1	0	0	1	1	0	1
		Solid State Devices and Integrated Circuits-II	3	3	2	1	1	0	0	1	1	0	1
		Signal Processing for VLSI	3	2	2	2	3	1	0	0	0	3	2
	Project Work Phase - I		3	3	3	3	3	2	2	3	2	3	2
IV	Project Work Phase - II		3	3	3	3	3	2	2	3	2	3	2

Mapping Criterion: Strong - 3 Significant - 2 Reasonable - 1

Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam - 603110

(An Autonomous Institution, Affiliated to Anna University, Chennai)

M.E. in VLSI DESIGN

REGULATIONS – 2018

CHOICE BASED CREDIT SYSTEM

I - IV SEMESTERS CURRICULUM AND SYLLABI

SEMESTER I

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	PMA1176	Advanced Applied Mathematics	FC	4	4	0	0	4
2	PVL1177	Digital CMOS VLSI Design	PC	5	3	0	2	4
3	PAE1176	Advanced Digital System Design	PC	3	3	0	0	3
4	PVL1176	Analog Integrated Circuit Design	PC	3	3	0	0	3
5	PVL1101	Solid State Devices and Integrated Circuits - I	PC	3	3	0	0	3
6	PVL1102	DSP Integrated Circuits	PC	3	3	0	0	3
PRACTICALS								
7	PVL1111	Integrated Circuits Laboratory	PC	4	0	0	4	2
8	PVL1115	Technical Seminar	EEC	2	0	0	2	1
			Total	**27**	**19**	**0**	**8**	**23**

SEMESTER II

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	PVL1201	Hardware Software Co-Design	PC	3	3	0	0	3
2	PVL1202	VLSI Physical Design and Algorithms	PC	5	3	0	2	4
3	PVL1203	Design for Testability	PC	3	3	0	0	3
4		Professional Elective - I	PE	3	3	0	0	3
5		Professional Elective - II	PE	3	3	0	0	3
6		Professional Elective - III	PE	5	3	0	2	4

PRACTICALS								
7	PVL1211	VLSI System Design Laboratory	PC	4	0	0	4	2
8	PVL1215	Technical Writing	EEC	2	0	0	2	1
			Total	**28**	**18**	**0**	**10**	**23**

SEMESTER III

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1		Professional Elective - IV	PE	3	3	0	0	3
2		Professional Elective - V	PE	3	3	0	0	3
3		Professional Elective - VI	PE	3	3	0	0	3
PRACTICALS								
4	PVL1318	Project Work Phase-I	EEC	12	0	0	12	6
			Total	**21**	**9**	**0**	**12**	**15**

SEMESTER IV

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
PRACTICALS								
1	PVL1418	Project Work Phase-II	EEC	24	0	0	24	12
			Total	**24**	**0**	**0**	**24**	**12**

TOTAL NO. OF CREDITS: 73

CATEGORIZATION OF COURSES

FOUNDATION COURSES (FC)

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	PMA1176	Advanced Applied Mathematics	FC	4	4	0	0	4
2	PVL1115	Technical Seminar	FC	2	0	0	2	1
3	PVL1215	Technical Writing	FC	2	0	0	2	1

PROFESSIONAL CORE (PC)

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	PVL1177	Digital CMOS VLSI Design	PC	5	3	0	2	4
2	PAE1176	Advanced Digital System Design	PC	3	3	0	0	3
3	PVL1176	Analog Integrated Circuit Design	PC	3	3	0	0	3
4	PVL1101	Solid State Devices and Integrated Circuits - I	PC	3	3	0	0	3
5	PVL1102	DSP Integrated Circuits	PC	3	3	0	0	3
6	PVL1201	Hardware Software Co-design	PC	3	3	0	0	3
7	PVL1202	VLSI Physical Design and Algorithms	PC	5	3	0	2	4
8	PVL1203	Design for Testability	PC	3	3	0	0	3
9	PVL1111	Integrated Circuits Laboratory	PC	4	0	0	4	2
10	PVL1211	VLSI System Design Laboratory	PC	4	0	0	4	2
			Total	**36**	**24**	**0**	**12**	**30**

EMPLOYABILITY ENHANCEMENT COURSE (EEC)

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1		Tech Club	EEC		1	0	1	1
2		IEEE professional society activities	EEC		0	0	2	1
3		Student Internal Funded Projects	EEC		0	0	2	1
4		Design Thinking	EEC		0	0	2	1
5		Internships	EEC		0	0	2	1

PROFESSIONAL ELECTIVES (PE)

SEMESTER II

ELECTIVE I

Sl. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	PAE1277	VLSI System Design	PE	3	3	0	0	3
2	PVL1276	Data Converters	PE	3	3	0	0	3
3	PVL1277	Signal Integrity for High Speed Design	PE	3	3	0	0	3
4	PVL1278	Microwave Integrated Circuits	PE	3	3	0	0	3

ELECTIVE II

Sl. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	PAE1276	Embedded System Design for IoT	PE	3	3	0	0	3
2	PCN1277	Multimedia compression techniques	PE	3	3	0	0	3
3	PCN1278	Software Defined Radio	PE	3	3	0	0	3
4	PCN1279	Cryptography and Network Security	PE	3	3	0	0	3

ELECTIVE III

Sl. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	PAE1278	MEMS and NEMS	PE	5	3	0	2	4
2	PAE1279	Nano Electronics and Technology	PE	5	3	0	2	4
3	PAE1281	DSP processor architecture and programming	PE	5	3	0	2	4
4	PAE1282	Advanced Digital Image Processing	PE	5	3	0	2	4

SEMESTER III

ELECTIVE IV

Sl. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	PAE1377	Advanced Computer Organization and Architecture	PE	3	3	0	0	3
2	PVL1321	CAD for VLSI IC Design	PE	3	3	0	0	3
3	PVL1376	RF IC Design	PE	3	3	0	0	3
4	PVL1377	Low Power VLSI Design	PE	3	3	0	0	3

ELECTIVE V

Sl. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	PVL1322	Scripting Languages for VLSI	PE	3	3	0	0	3
2	PVL1323	VLSI Technology	PE	3	3	0	0	3
3	PVL1324	Nano Scale Transistors	PE	3	3	0	0	3
4	PAE1177	Sensors, Actuators and System Interface	PE	3	3	0	0	3

ELECTIVE VI

Sl. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	PVL1325	Artificial Intelligence	PE	3	3	0	0	3
2	PVL1326	Quantum Computing and Quantum Information	PE	3	3	0	0	3
3	PVL1327	Solid State Devices and Integrated Circuits-II	PE	3	3	0	0	3
4	PVL1378	Signal Processing for VLSI	PE	3	3	0	0	3

DISTRIBUTION OF CREDITS

Sl. No	Category	Credits as per Semester				Total Credits	Percentage
		I	II	III	IV		
1	FC	4				4	5.5%
2	PC	18	12			30	41.1%
3	EEC	1	1	6	12	20	27.4%
4	PE		10	9		19	26%
		23	23	15	12	73	